FOENIX RETRO SYSTEMS

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Core2x F256Jr2/K2
Short Form Documentation
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Updated MMU MEMORY CONTROL

MMU Model Address Offset: $0000
Extended Model Address Offset: $000000

$0000 - $000000: MMU Memory Control Register
---
bit[0] - Active MMU LUT[0]
bit[1] - Active MMU LUT[1]
bit[2] - Not Used
bit[3] - SRAM Accessible in Exteded Mode (24bits Address)
bit[4] - Edit MMU LUT[0]
bit[5] - Edit MMU LUT[1]
bit[6] - Not Used
bit[7] - Edit MMU Enable

Updated IO MEMORY CONTROL

MMU Model Address Offset: $0001
Extended Model Address Offset: $000001

$0001 - $000001: IO Memory Control Register
---
bit[0] - Active IO PAGE[0]
bit[1] - Active IO PAGE[1]
bit[2] - IO Page Disable - 0 = Enabled, 1 = Disabled
bit[3] - Active IO PAGE[2]
bit[4] - Move Decoding of IO Devices to High-Memory
bit[5] - Move Decoding of Flash/Cart to High-Memory
bit[6] - Sprites Block Select - 0: Sprite 0-63, 1: Sprite 64-127
bit[7] - Not Used

IOPAGE[2:0]
000: GAMMA Table, Mouse Graphics, All IO Devices & Vicky Registers
001: Block Text FONT0 & 1, GRAPHICS COLOR LUT 0,1,2,3
010: Block Text Character Memory
011: Block Text Color Memory
100: Memory Text Color Background LUT 0 & 1, Foreground LUT 0 & 1
101: Memory Text FONT 0,1,2,3 for 8x8, or 0,1 for 8x16
110: Not Used
111: Not Used

NEW MMU PAGE 0 Extension Bit to Access 2M SRAM

MMU Model Address Offset: $0002 & $0003

Extended Model Address Offset: $000002 & $000003

$0002 - $000002: MMU PAGE 0 Extension Bit 0 to 3

---

bit[0] - LUT0[0][8]
bit[1] - LUT0[0][9]
bit[2] - LUT0[1][8]
bit[3] - LUT0[1][9]
bit[4] - LUT0[2][8]
bit[5] - LUT0[2][9]
bit[6] - LUT0[3][8]
bit[7] - LUT0[3][9]

$0003 - $000003: MMU PAGE 0 Extension Bit 4 to 7

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bit[0] - LUT0[4][8]
bit[1] - LUT0[4][9]
bit[2] - LUT0[5][8]
bit[3] - LUT0[5][9]
bit[4] - LUT0[6][8]
bit[5] - LUT0[6][9]
bit[6] - LUT0[7][8]
bit[7] - LUT0[7][9]

Extended Address Decoding

$00_0000 - $07_FFFF - 512K SRAM Default RAM (Page 0)
$08_0000 - $0F_FFFF - 512K FLASH
$10_0000 - $13_FFFF - 256K CARTRIDGE
$14_0000 - $1F_FFFF - 768K NOTHING HERE
$20_0000 - $27_FFFF - 512K SYSTEM SRAM Page 1
$40_0000 - $47_FFFF - 512K SYSTEM SRAM Page 2
$60_0000 - $67_FFFF - 512K SYSTEM SRAM Page 3

Updated VDMA Controller

MMU Model Address Offset: $DF00

Extended Model Address Offset: $F01F00

```
$DF00 - $F01F00:    Control Register
$DF01 - $F01F01:    8bits Mode Fill Byte
$DF02 - $F01F02:    16bits Mode Fill Byte (Low)
$DF03 - $F01F03:    16bits Mode Fill Byte (Hi)
$DF04 - $F01F04:    SOURCE ADDRESS (Low)
$DF05 - $F01F05:    SOURCE ADDRESS (Mid)
$DF06 - $F01F06:    SOURCE ADDRESS (Hi)
$DF07 - $F01F07:    RESERVED
$DF08 - $F01F08:    DESTINATION ADDRESS (Low)
$DF09 - $F01F09:    DESTINATION ADDRESS (Mid)
$DF0A - $F01F0A:    DESTINATION ADDRESS (Hi)
$DF0B - $F01F0B:    RESERVED
$DF0C - $F01F0C:    1D Mode - Size (Low) - 2D Mode - Size X (Low)
$DF0D - $F01F0D:    1D Mode - Size (Mid) - 2D Mode - Size X (Hi)
$DF0E - $F01F0E:    1D Mode - Size (Hi)  - 2D Mode - Size Y (Low)
$DF0F - $F01F0F:    1D Mode - Not Used   - 2D Mode - Size Y (Hi)
$DF10 - $F01F10:    STRIDE X (Low)
$DF11 - $F01F11:    STRIDE X (Hi)
$DF12 - $F01F12:    STRIDE X (Low)
$DF13 - $F01F13:    STRIDE X (Hi)

$DF00 - $F01F00:    Control Registers bit Definition
-------------------------------------------------------------
bit[0] - Enable DMA Controller
bit[1] - Mode (1D/2D) - 0 = 1D, 1 = 2D
bit[2] - Fill Mode - 0 = Normal Transfer, 1 = Fill Destination
bit[3] - Not Used
bit[4] - Data Mask (Low) (When in 16bits Mode) (1 = Mask Byte)
bit[5] - Data Mask (Hi)  (When in 16bits Mode) (1 = Mask Byte)
bit[6] - 16bits Transfer/Fill Mode
bit[7] - Start Transfer
```

NEW Memory Text Controller

MMU Model Address Offset: $D300
Extended Model Address Offset: $F01300

```
$D300 - $F01300:    Memory Text Control Register
$D301 - $F01301:    Cursor Control Register
$D302 - $F01302:    Cursor X Position
$D303 - $F01303:    Cursor Y Position
$D304 - $F01304:    START TEXT ADDRESS (Low) [Even Address]
$D305 - $F01305:    START TEXT ADDRESS (Mid)
$D306 - $F01306:    START TEXT ADDRESS (Hi)
$D307 - $F01307:    RESERVED - (PRECHARGE VALUE 0x0A)
$D308 - $F01308:    START COLOR ADDRESS (Low) [Even Address]
$D309 - $F01309:    START COLOR ADDRESS (Mid)
$D30A - $F0130A:    START COLOR ADDRESS (Hi)
$D30B - $F0130B:    RESERVED
$D30C - $F0130C:    RESERVED
$D30D - $F0130D:    CURSOR COLOR B
$D30E - $F0130E:    CURSOR COLOR G
$D30F - $F0130F:    CURSOR COLOR R
$D310 - $F01310:    Cursor Graphic Line 0 (x8/x16)(TOP)
$D311 - $F01311:    Cursor Graphic Line 1 (x8/x16)
$D312 - $F01312:    Cursor Graphic Line 2 (x8/x16)
$D313 - $F01313:    Cursor Graphic Line 3 (x8/x16)
$D314 - $F01314:    Cursor Graphic Line 4 (x8/x16)
$D315 - $F01315:    Cursor Graphic Line 5 (x8/x16)
$D316 - $F01316:    Cursor Graphic Line 6 (x8/x16)
$D317 - $F01317:    Cursor Graphic Line 7 (x8/x16)(BOTTOM8)
$D318 - $F01318:    Cursor Graphic Line 8  (x16)
$D319 - $F01319:    Cursor Graphic Line 9  (x16)
$D31A - $F0131A:    Cursor Graphic Line 10 (x16)
$D31B - $F0131B:    Cursor Graphic Line 11 (x16)
$D31C - $F0131C:    Cursor Graphic Line 12 (x16)
$D31D - $F0131D:    Cursor Graphic Line 13 (x16)
$D31E - $F0131E:    Cursor Graphic Line 14 (x16)
$D31F - $F0131F:    Cursor Graphic Line 15 (x16) (BOTTOM16)
```

NEW LUT TABLE FOR FG/BG Colors

MMU Model Address Offset: $C000 (IO Page 4)
Extended Model Address Offset: $F08000

NEW FONT Memory (4x BANKS of 8x8) or (2x BANKS of 8x16)

MMU Model Address Offset: $C000 (IO Page 5)
Extended Model Address Offset: $F0A000

$D300 - $F01300:   Memory Text Control Register
---
bit[0] - Memory Text Mode Enable
bit[1] - Mode (8/16) - 0 = 8x8 Mode, 1 = 8x16 Mode
bit[2] - Not Used (Reserved)
bit[3] - Not Used (Reserved)
bit[4] - Not Used (Reserved)
bit[5] - Not Used (Reserved)
bit[6] - Not Used (Reserved)
bit[7] - Not Used (Reserved)

$D301 - $F01301:   Cursor Control Register
---
bit[0] - Cursor Enable
bit[1] - Cursor Flash Rate[0] - Independent Flash Rate from Normal Cursor
bit[2] - Cursor Flash Rate[1] - Independent Flash Rate from Normal Cursor
bit[3] - Cursor Flashing Not - 0 = Flashing, 1 = Not Flashing
bit[4] - Text Flash Rate[0]
bit[5] - Text Flash Rate[1]
bit[6] - FONT Size - 0 = 8x8, 1 = 8x16
bit[7] - Not Used (Reserved)

Flash Rate[1:0]:

00: 1 Flash Per Second
01: 2 Flashes Per Second
10: 4 Flashes Per Second
11: 5 Flashes Per Second

TEXT SCREEN 16bits Definition

[7:0]   ASCII CHARACTER
[8]   ATTRIBUTE - FONT BANK SELECT[0] (8x8 Mode Only)
[9]   ATTRIBUTE - FONT BANK SELECT[1] (8x8/8x16 Mode)
[10]   FOREGROUND LUT[0] Choice
[11]   BACKGROUND LUT[1] Choice
[12]   ATTRIBUTE - FONT INVERSION ENABLE
[13]   ATTRIBUTE - FONT FLASHING ENABLE
[14]   Not Used (Reserved)
[15]   Not Used (Reserved)

COLOR SCREEN 16bits Definition

[7:0]   BACKGROUND COLOR 1 Byte Color Against the LUT
[15:8]   FOREGROUND COLOR 1 Byte Color Against the LUT

Updated VICKY Master Control Register

MMU Model Address Offset: $D000

Extended Model Address Offset: $F01000

$D000 - $F01000: VICKY MASTER CONTROL REG 0

---

bit[0] - Text Mode Enable (Block Text Mode)
bit[1] - Text Mode Overlay Enable (Block Text Mode)
bit[2] - Graphics Mode Enable
bit[3] - Bitmap Enable
bit[4] - Tilemap Enable
bit[5] - Sprite Enable
bit[6] - Enable GAMMA Correction
bit[7] - Disable Video (Turn Off VICKY Scan of Memory)

$D001 - $F01001: VICKY MASTER CONTROL REG 1

---

bit[0] - Video Mode[0]
bit[1] - Video Mode[1]
bit[2] - Video Mode[2]
bit[3] - Turn Sync Off (Put Monitor in Sleep Mode)
bit[4] - Show Background in Overlay Mode When BG Color = 0
bit[5] - Select Font Bank
bit[6] - Text Memory Mode Enable (Take Precedence over Block Text)
bit[7] - Text Memory Mode Show BG in Overlay Mode When BG = 0

$D00A - $F0100A: VICKY MASTER CONTROL REG 2 (Extended)

---

bit[0] - DrawLine Enable
bit[1] - Not Used (Reserved)
bit[2] - Not Used (Reserved)
bit[3] - Not Used (Reserved)
bit[4] - Not Used (Reserved)
bit[5] - Not Used (Reserved)
bit[6] - Not Used (Reserved)
bit[7] - Not Used (Reserved)

NEW VICKY Draw Line Registers

MMU Model Address Offset: $D180

Extended Model Address Offset: $F01180

```
$D180 - $F01180:    Drawline Control Register
$D181 - $F01181:    Line Color (LUT Byte)
$D182 - $F01182:    (Write)   Line X0 (Low)
$D183 - $F01183:    (Write)   Line X0 (Hi)
$D182 - $F01182:    (Read)    FIFO Data Count[7:0]
$D183 - $F01183:    (Read)    FIFO Data Count[12:8]
$D184 - $F01184:    Line X1 (Low)
$D185 - $F01185:    Line X1 (Hi)
$D186 - $F01186:    Line Y0
$D187 - $F01187:    Line Y1


$D180 - $F01180:    Draw line Control Register (Write)
-------------------------------------------------------------
bit[0] - Line Draw Enable
bit[1] - Go Start To Draw
bit[2] - Bitmap Layer Choice[0]
bit[3] - Bitmap Layer Choice[1]
bit[4] - Reset
bit[5] - Not Used (Reserved)
bit[6] - Not Used (Reserved)
bit[7] - Not Used (Reserved)

$D180 - $F01180:    Draw line Control Register (Read)
-------------------------------------------------------------
bit[0] - Line Draw Enable
bit[1] - Go Start To Draw
bit[2] - Bitmap Layer Choice[0]
bit[3] - Bitmap Layer Choice[1]
bit[4] - Reset
bit[5] - Not Used (Reserved)
bit[6] - Not Used (Reserved)
bit[7] - LineDraw Busy Flag (wait to return to 0 )
```

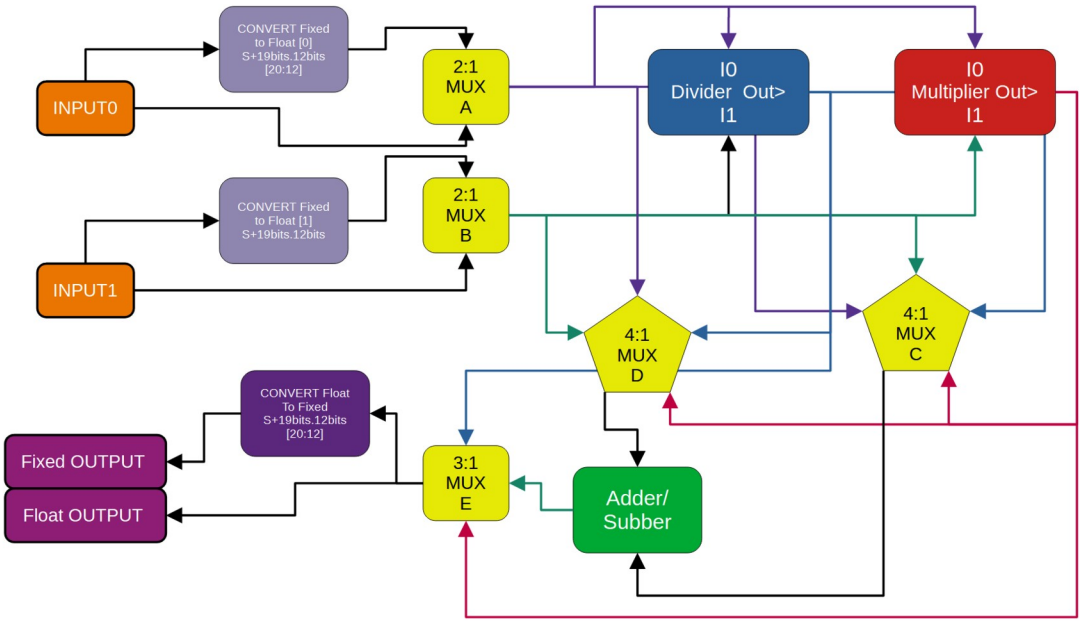
BASIC Example:

```
1000  proc hwline(x0,y0,x1,y1,col)
1005  ?$D00A=1:?$D180=1:pokew $D182,0
1010  ?$D181=col:pokew $D182,x0:pokew $D184,x1
1020  ?$D186=y0:?$D187=y1
1030  ?$D180=3
1040  while (?$D180&$80)<>$80:wend
1045  ?$D00A=0
1050  endproc
```

NEW Floating-Point Module

MMU Model Address Offset: $DE80

Extended Model Address Offset: $F01E80



[Write]

$DE80 - $F01E80: FP Math Block Control Register 0
$DE81 - $F01E81: FP Math Block Control Register 1
$DE82 - $F01E82: FP Math Block Control Register 2
$DE82 - $F01E82: FP Math Block Control Register 3
$DE84 - $F01E84: Not Used (Reserved)
$DE85 - $F01E85: Not Used (Reserved)
$DE86 - $F01E86: Not Used (Reserved)
$DE87 - $F01E87: Not Used (Reserved)
$DE88 - $F01E88: User Input 0 (LL)
$DE89 - $F01E89: User Input 0 (LH)
$DE8A - $F01E8A: User Input 0 (HL)
$DE8B - $F01E8B: User Input 0 (HH)
$DE8C - $F01E8C: User Input 1 (LL)
$DE8D - $F01E8D: User Input 1 (LH)
$DE8E - $F01E8E: User Input 1 (HL)
$DE8F - $F01E8F: User Input 1 (HH)

User Input 0

Either a S.19.12 Format or IEEE 32bits Floating-Point Format S.8.23

User Input 1

Either a S.19.12 Format or IEEE 32bits Floating-Point Format S.8.23

$DE80 - $F01E80: FP Math Block Control Register 0
---
bit[0] - User Input 0 Select - 0 = FP Input, 1 = Converted
bit[1] - User Input 1 Select - 0 = FP Input, 1 = Converted
bit[2] - Not Used (Reserved)
bit[3] - Addition/Substraction - 0 = Addition, 1 = Substraction
bit[4] - ADDER/SUBBER Input 0 MUX[0]
bit[5] - ADDER/SUBBER Input 0 MUX[1]
bit[6] - ADDER/SUBBER Input 1 MUX[0]
bit[7] - ADDER/SUBBER Input 1 MUX[1]

ADDER/SUBBER MUX[1:0]
00: Converter Output 0 (Fix to Float Converter or FP Direct Input)
01: Converter Output 1 (Fix to Float Converter or FP Direct Input)
10: FP Mutliplier Output
11: FP Divisor Output

$DE81 - $F01E81: FP Math Block Control Register 1
---
bit[0] - OUTPUT MUX[0]
bit[1] - OUTPUT MUX[1]
bit[2] - Not Used (Reserved)
bit[3] - Not Used (Reserved)
bit[4] - Not Used (Reserved)
bit[5] - Not Used (Reserved)
bit[6] - Not Used (Reserved)
bit[7] - Not Used (Reserved)

OUTPUT MUX[1:0]
00: Multiplier Output
01: Divisor Output
10: Adder/Subber Output
11: FP 1.0 Output ($3F800000)

$DE82 - $F01E82: FP Math Block Control Register 2
---
bit[0] - Converter Input 0 - Tvalid (i.e. Enable)
bit[1] - Direct Input 0 - Tvalid (i.e. Enable)
bit[2] - Converter Input 1 - Tvalid (i.e. Enable)
bit[3] - Direct Input 1 - Tvalid (i.e. Enable)
bit[4] - Not Used (Reserved)
bit[5] - Not Used (Reserved)
bit[6] - Not Used (Reserved)
bit[7] - Not Used (Reserved)

$DE83 - $F01E83: FP Math Block Control Register 3
---
bit[0] - Not Used (Reserved)
bit[1] - Not Used (Reserved)
bit[2] - Not Used (Reserved)
bit[3] - Not Used (Reserved)
bit[4] - Not Used (Reserved)
bit[5] - Not Used (Reserved)
bit[6] - Not Used (Reserved)
bit[7] - Not Used (Reserved)

(Read)
$DE80 - $F01E80: FP Math Block Control Register 0
$DE81 - $F01E81: FP Math Block Control Register 1
$DE82 - $F01E82: FP Math Block Control Register 2
$DE82 - $F01E82: FP Math Block Control Register 3
$DE84 - $F01E84: Multiplier Module Status Output
$DE85 - $F01E85: Diviser Module Status Output
$DE86 - $F01E86: Adder/Subber Module Status Output
$DE87 - $F01E87: Converter Module Status Output
$DE88 - $F01E88: Output Mux Output (LL) (Floating Point)
$DE89 - $F01E89: Output Mux Output (LH) (Floating Point)
$DE8A - $F01E8A: Output Mux Output (HL) (Floating Point)
$DE8B - $F01E8B: Output Mux Output (HH) (Floating Point)
$DE8C - $F01E8C: Output Fixed Converter (LL)
$DE8D - $F01E8D: Output Fixed Converter (LH)
$DE8E - $F01E8E: Output Fixed Converter (HL)
$DE8F - $F01E8F: Output Fixed Converter (HH)

$DE84 - $F01E84: FP Multiplier Status Register
---
bit[0] - NAN (Not a Number)
bit[1] - Overflow
bit[2] - Underflow
bit[3] - Zero
bit[4] - Output Valid
bit[5] - Not Used (Reserved)
bit[6] - Not Used (Reserved)
bit[7] - Not Used (Reserved)

$DE85 - $F01E85: FP Divisor Status Register
---
bit[0] - NAN (Not a Number)
bit[1] - Overflow
bit[2] - Underflow
bit[3] - Zero
bit[4] - Division by Zero
bit[5] - Output Valid
bit[6] - Not Used (Reserved)
bit[7] - Not Used (Reserved)

$DE86 - $F01E86: FP Adder/Subber Status Register
---
bit[0] - NAN (Not a Number)
bit[1] - Overflow
bit[2] - Underflow
bit[3] - Zero
bit[4] - Output Valid
bit[5] - Not Used (Reserved)
bit[6] - Not Used (Reserved)
bit[7] - Not Used (Reserved)

$DE87 - $F01E87: FP Converter (FP 2 Fixed) Status Register
---
bit[0] - Not Used (Reserved)
bit[1] - Overflow
bit[2] - Underflow
bit[3] - Output Valid
bit[4] - Not Used (Reserved)
bit[5] - Not Used (Reserved)
bit[6] - Not Used (Reserved)
bit[7] - Not Used (Reserved)